# A Silicon MOS MMIC Upconverter for CATV Applications

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**Abstract** We present the design and performance of a new silicon MOS upconverter designed for use in CATV tuners and related components. The upconverter contains a double balanced mixer, a VCO, and a buffer amplifier. It converts frequencies in the CATV band from 50 - 860 MHz to an IF in the range of 1000 - 1250 MHz. The silicon upconverter is an economical alternative to GaAs parts, and shows comparable performance.

## Introduction

In this paper we describe the design and performance of a silicon MOS upconverter for a CATV dual-conversion analog/digital tuner module. The tuner is designed to accept up to 128 cable signals in the 50 - 860 MHz range, and convert up to a first IF in the range of 1100 - 1500 MHz. After this upconversion, the signal is filtered and amplified, and then downconverted to 40 Mhz in subsequent circuit blocks. A block diagram of a typical tuner system is shown in Figure 1. The phase locked loops and related frequency control elements are not shown.

Because there is no preselection in this system, the upconverter must exhibit low second and third order IM distortion, as well as low noise figure. Also, since the tuner must be compatible with digital modulation, the phase noise on the LO VCO must be low. Similar circuits have been made using GaAs MESFET technology [1], [2], but to the author's knowledge, the design presented here is the first application of silicon MOS technology to this problem.

## Circuit Design

Specifications for the upconverter are shown in Table 1. These are not all of the specs, but rather represent the more significant design challenges for the circuits.

As mentioned above, the 2nd and 3rd order intermodulation distortion for the upconverter must be low. According to CATV practice,

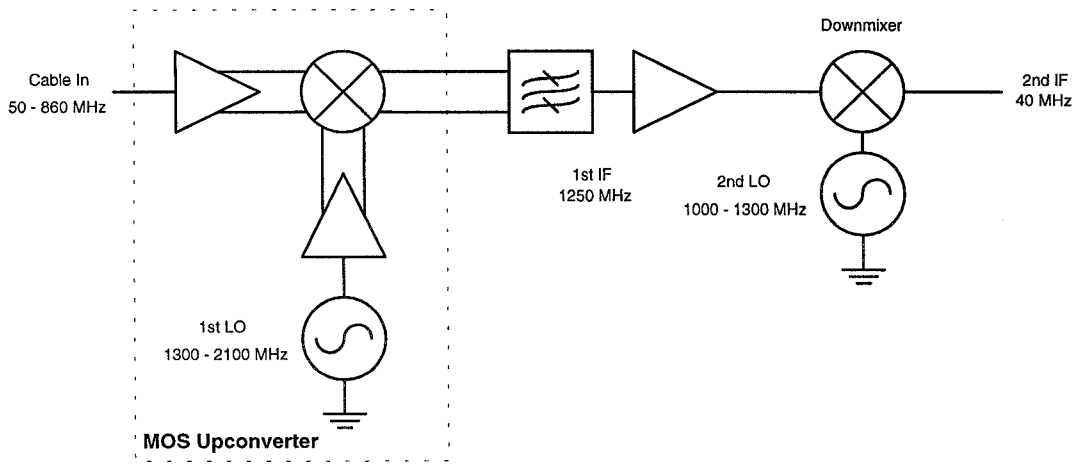


**Figure 1. Block Diagram of the CATV tuner.**

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these are measured by applying all of the 128 carriers to the input of the circuit and measuring composite triple beat (CTB) and composite second order (CSO) levels. However, it is very difficult to simulate this performance using CAD methods, due to the number of signal tones. Using harmonic balance simulators, such as Hewlett Packard's MDS, it is much easier to simulate the two tone distortion products. The design approach taken was to compute the required IM performance in terms of two-tone distortion, and design the circuits to the resulting two-tone limits.

| | |
|---|---|
| RF range | 50 - 860 MHz |
| IF range | 1100 - 1400 MHz |
| LO range | 1150 - 2260 MHz |
| Tuning voltage | 0.5 - 28 V |
| gain | 3 - 7 dB |
| noise figure | 8.8 dB |
| Input 3rd order intercept | +10 dBm |
| Input 2nd order intercept | +40 dBm |
| VCO phase noise | -75 dBc/Hz @ 10 kHz |

**Table 1. Performance Specifications for MOS upconverter.**

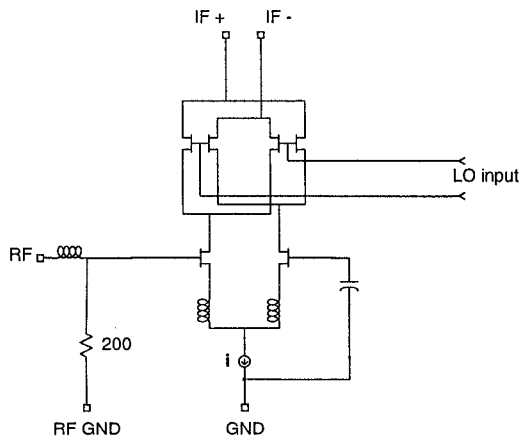


**Figure 2. MOSFET Gilbert Cell mixer.**

The LNA/Mixer design chosen was a MOSFET Gilbert Cell as shown in Figure 2. This topology provides good broadband noise and intermod performance. For broadband matching, a shunt resistor was placed on the rf input. Source degeneration inductors improved noise figure and intermod performance of the rf difpair.

The balanced mixer provides a differential output which must be combined off chip.

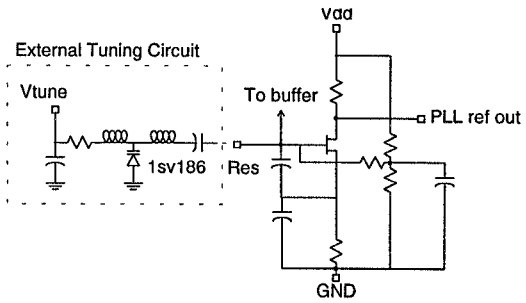


**Figure 3. VCO and external tank circuit.**

This may be easily accomplished using a transformer or rat race ring.

VCO phase noise is a critical parameter for the downconverter, especially for digital applications. No attempt was made to simulate of VCO phase noise, given its strong dependence on package parasitics and the external varactor performance. Instead, an empirical approach was taken.

The circuit design chosen was a Clapp oscillator, shown in Figure 3, feeding a differential buffer amplifier, shown in Figure 4. An external varactor in the VCO tank circuit was used to achieve the broad tuning range required.

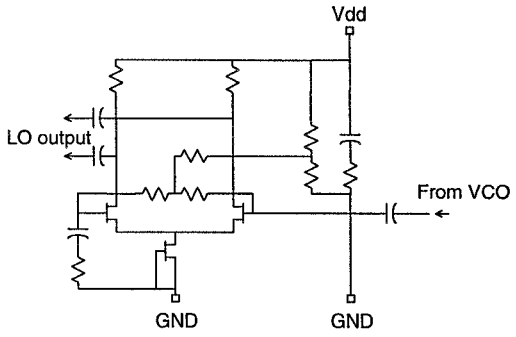


**Figure 4. LO buffer amp.**

The upconverter chips was designed using the HP MDS circuit simulator. The active devices were modeled using the HP Root model. Circuits were fabricated using Motorola's RFGCMOS IC technology [3]. This process is based on a low cost VLSI technology with the addition of fully integrated passive components and MOSFETs optimized for RF circuit applications [4]

The upconverter is designed to be packaged in a low cost SO16 package, however, the results shown here are for die tested in hybrid test fixtures. Die size is 34 x 65 mils.

## Test

Test of the upconverter is somewhat problematic, since the test results depend strongly on the circuit in which the device is operating. For example, the off-chip VCO tank circuit is critical to the tuning range and phase noise of the VCO. More importantly, the output combining network has a large effect on the intermodulation distortion of the converter.

Die were bonded into hybrid test fixtures for the measurements shown here. The balanced outputs of the mixer were combined using a transmission line transformer, along with blocking caps and rf chokes.

Measured data of gain, noise figure, and IIP3 are shown in Figures 5 through 7. The data were taken at a fixed IF of 1250 MHz, so the LO tuning range was 1300 - 2110 MHz. The noise figure data at 50 MHz IF is not shown due to difficulty with the test at that frequency.

Input 3rd order intercept point was measured at +9.9 dBm worst case across the band. Input 2nd order intercept point worst case was +37 dBm. Both these results are slightly below specification.

Phase noise was measured using a PLL with a locking bandwidth of approximately 1 Hz, so that the results are essentially the open loop values. The PLL limited the measurements to tune voltages below about 8.5 V. Experience has shown that the worst case phase noise occurs at the low end of the tuning range, due to the steep slope of the varactor C vs. V at that point.

The phase noise was found to be a function primarily of the tuning voltage on the varactor, Varactor voltages below about 1.5 V caused the phase noise to increase to values above -81 dBc/Hz @ 10 kHz offset. Worst case phase noise occurred at the low tune voltage of 0.4 V and was -77.5 dBc/Hz @ 10 kHz. Above 2V tuning voltage and 1400 Mhz, the phase noise dropped to better than -82 dBc/Hz @ 10 kHz offset.

The IC drew 115 mA from a 9 V supply.

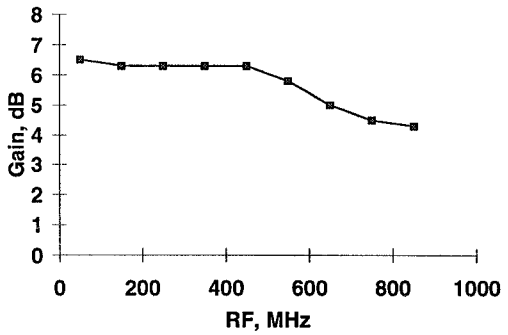


**Figure 5. Gain vs. input frequency**

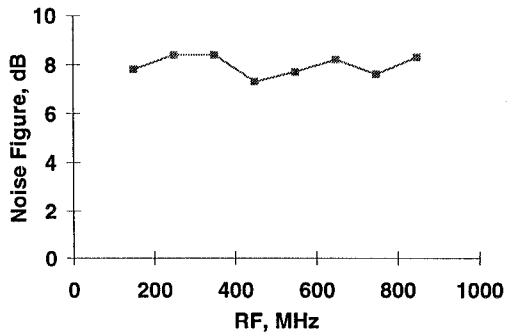


**Figure 6. Noise figure vs. input frequency**

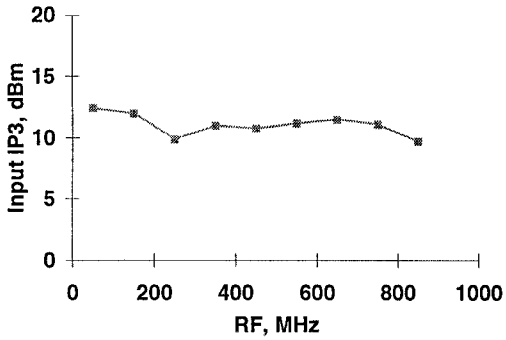


**Figure 7. Input intercept point vs. frequency**

## Conclusions

A broadband upconverter suitable for CATV tuner applications has been described. The tuner exhibits low noise, high IP3, and conversion gain over the 50 - 860 MHz CATV band. The silicon downconverter is an economical alternative to GaAs parts, and shows comparable performance.

## Acknowledgments

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## References

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